SOME SCIENTIFIC APPLICATIONS OF THE 803-B

Science

University of Abardeen
University of Exeter
University of Reading
University of Hull
University of Leicester
Technical University of Helsinki
Brunel College of Technology
Bristol College of Science and Technology
TNO IWECO Institute (Delft)
Technische Hochschule (Darmstadt)
Birmingham College of Advanced Technology
University of Wroclaw (Poland)

Mullard Ltd. — Research Lab. (Salfords)
Royal Radar Establishment (Worcestershire)

Engineering

G. P. O. Research Station — London
Philipp Holzmann A. G. — Frankfurt
Electrotechnical Institute — Warsaw
Koch & Mazzucki — Hannover
The Lummus Co. Ltd. — London
Mullard Ltd. — Laboratory — Southampton

Fairey Aviation Div. Aircraft Ltd. — Hayes

De Havilland Aircraft Co. Ltd. — London

Lummus Company Inc. — N. York

United Kingdom Atomic Energy Authority — Calder Hall
Brush Electrical Engineering Co. Ltd. — Loughborough

NCR

THE NATIONAL CASH REGISTER CO. OF PORTUGAL, S. A. R. L.

Av. do Brasil, 56, 3.º – Telef. 76 60 41/7 – LISBOA 5

NCR

SCIENTIFIC APPLICATIONS OF THE ELLIOTT 803-B ELECTRONIC COMPUTER

LABORATÓRIO NACIONAL DE ENGENHARIA CIVIL

SEP. 16 - OCT. 6
1962

1620 CHARACTER CODING

Alphameric Character	Input			Core Storage		Output		
	Typewriter	Tape	Card	Alpha	Num	Typewriter	Tape	Card
(Blank)	(Space)	C	(Blank)	C	C	(Space)	C	(Blank)
. (Period)	.	X0821	12, 3, 8	C	3	.	X0821	12, 3, 8
)	)	X0C84	12, 4, 8	C	4	)	X0C84	12, 4, 8
+	+	X0C	12	1	C	+	X0C	12
$	$	XC821	11, 3, 8	1	3	$	XC821	11, 3, 8
*	*	X84	11, 8, 4	1	4	*	X84	11, 4, 8
- (Hyphen)	-	X	11	2	C	-	X	11
/	/	0C1	0, 1	2	1	/	0C1	0, 1
, (Comma)	,	0C821	0, 3, 8	2	3	,	0C821	0, 3, 8
(	(	084	0, 4, 8	2	4	(	084	0, 4, 8
=	=	821	3, 8	3	3	=	821	3, 8
@	@	C84	4, 8	3	4	@	C84	4, 8
A-I	A-I	X0, 1-9	12, 1-9	4	1-9	A-I	X0, 1-9	12, 1-9
0 (-)	(None)	(None)	11, 0	5	C	- (Hyphen)	X	11, 0
J-R	J-R	X, 1-9	11, 1-9	5	1-9	J-R	X, 1-9	11, 1-9
1-9 (-)	J-R	X, 1-9	11, 1-9	5	1-9	J-R	X, 1-9	11, 1-9
S-Z	S-Z	0, 2-9	0, 2-9	6	2-9	S-Z	0, 2-9	0, 2-9
0 (+)	0	0	0 or 12, 0	7	C	0	0	0
1-9 (+)	1-9	1-9	1-9	7	1-9	1-9	1-9	1-9
‡	‡	082	0, 2, 8	C	C28	(Stop)	EOL	0, 2, 8
Numerical Character								
(Blank)	(Space)	C	(Blank)		C	0	0	0
0 (+)	0	0	0		C	0	0	0
0 (-)	$\bar{0}$	X, X0C	11, 0		F	$\bar{0}$	X	11, 0
1-9 (+)	1-9	1-9	1-9		1-9	1-9	1-9	1-9
1-9 (-)	$\bar{1}$-$\bar{9}$	X, 1-9	11, 1-9		J-$\bar{R}$	J-$\bar{R}$	X, 1-9	11, 1-9
‡	‡	082	0, 2, 8		C82	(Stop, WN) ‡ (DN)	EOL(WN) 082 (DN)	0, 2, 8
Num Blank †	@	C84	4, 8		C84	@	C84	(Blank)

† For Card Format Use Only

ALLOWABLE INDIRECT ADDRESSING

Arithmetic Instructions:	MNEMONIC	CODE	P & Q	P
Add	A	21	X	
Add Immediate	AM	11		X
Subtract	S	22	X	
Subtract Immediate	SM	12		X
Multiply	M	23	X	
Multiply Immediate	MM	13		X
Load Dividend	LD	28	X	
Load Dividend Immediate	LDM	18		X
Divide	D	29	X	
Divide Immediate	DM	19		X
Internal Data Transmission Instructions:				
Transmit Digit	TD	25	X	
Transmit Digit Immediate	TDM	15		X
Transmit Field	TF	26	X	
Transmit Field Immediate	TFM	16		X
Transmit Record	TR	31	X	
Transfer Numerical Strip	TNS	72	X	
Transfer Numerical Fill	TNF	73	X	
Logic (Compare and Branch) Instructions:				
Compare	C	24	X	
Compare Immediate	CM	14		X
Branch	B	40		X
Branch No Flag	BNF	44	X	
Branch No Record Mark	BNR	45	X	
Branch On Digit	BD	43	X	
Branch Indicator	BI	46		X
Branch No Indicator	BNI	47		X
Branch and Transmit	BT	27	X	
Branch and Transmit Immediate	BTM	17		X
Branch Back	BB	42		
Input-Output Instructions:				
Read Numerically	RN	36		X
Write Numerically	WN	38		X
Dump Numerically	DN	35		X
Read Alphamerically	RA	37		X
Write Alphamerically	WA	39		X
Control	K	34		
Program Control Instructions:				
Set Flag	SF	32		X
Clear Flag	CF	33		X
Move Flag	MF	71	X	
Halt	H	48		
No Operation	NOP	41		

1620 STORAGE REGISTERS

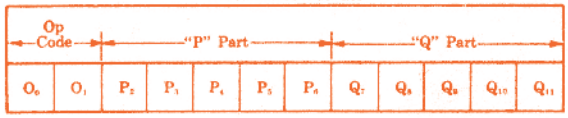
Register	Function
IR-1	Contains address of next instruction if machine is stopped with stop key or halt instruction.
IR-2	Saves return address when BT and BTM instructions are executed.
OR-1	Contains Q address after 1-cycle of an instruction.
OR-2	Contains P address after 1-cycle of an instruction.
OR-3	Retains address of low-order multiplier digit during multiplication.
PR-1	Saves return address when a save key operation occurs. Decremented for each new multiply digit during multiply.
PR-2	Decremented for each new multiplicand digit during multiply.
PR-3	Used to add partial product to each multiply cycle result.
MAR	Addresses core storage.
MBR	Receives digits entering or leaving core storage.
MDR	Receives addressed digit entering or leaving core storage.
Digit	Stores partial product during multiplication.
OP	Contains OP code of instruction just executed if machine is stopped with stop key or halt instruction.
Multiplier	Contains multiplier digits during multiply operation.
Sense & Branch	Contains I/O device code during input/output operations. Units positions used to develop each quotient digit during divide operation.
Digit & Branch	On some machines, combines functions of Digit, Sense & Branch Registers.

SIGNIFICANCE OF P & Q ADDRESS

Operation Code	P Address	Q Address
11—Add (I)*	Memory address of units position of Augend.	Q_{11} of instruction is units position of Addend.
21—Add	Same as Code 11.	Memory address of units position of Addend.
12—Subtract (I)*	Memory address of units position of Minuend.	Q_{11} of instruction is units position of Subtrahend.
22—Subtract	Same as Code 12.	Memory address of units position of Subtrahend.
13—Multiply (I)*	Memory address of units position of Multiplicand.	Q_1 of instruction is units position of Multiplier.
23—Multiply	Same as Code 13.	Memory address of units position of Multiplier.
14—Compare (I)*	Memory address of units position of the field to which another field is to be compared.	Q_{11} of instruction is units position of the field to be compared with the field at the P address.
24—Compare	Same as Code 14.	Memory address of units position of the field to be compared with the field at the P address.
15—Transmit Digit (I)*	Memory address to which single digit is to be transmitted.	Q_{11} of instruction is the single digit to be transmitted.
25—Transmit Digit	Same as Code 15.	Memory address of single digit to be transmitted.
16—Transmit Field (I)*	Memory address to which units position of field is to be transmitted.	Q_{11} of instruction is the units position of the field to be transmitted.
26—Transmit Field	Same as Code 16.	Memory address of units position of the field to be transmitted.
17—Branch and Transmit (I)*	"P minus one" is the memory address to which the units position of the Q field is to be transmitted. "P" is the memory address of the high-order digit of the next instruction to be interpreted and executed.	Q_{11} of instruction is the units position of the field to be transmitted.
27—Branch and Transmit	Same as Code 17.	Memory address of units position of the field to be transmitted.
18—Load Dividend (I)*	Memory address in Product Area to which units position of field (Dividend) is to be transmitted.	Q_{11} of instruction is the units position of the field (Dividend) to be transmitted.
28—Load Dividend	Same as Code 18.	Memory address of the units position of the field (Dividend) to be transmitted.
19—Divide (I)*	Memory address at which first subtraction of the Divisor is to occur.	Q_{11} of instruction is the units position of the Divisor.
29—Divide	Same as Code 19.	Memory address of units position of Divisor.
31—Transmit Record	Memory address to which high-order position of record is to be transmitted.	Memory address of high-order position of the record to be transmitted.
32—Set Flag	Memory address at which flag bit is to be placed.	Not used.
33—Clear Flag	Memory address from which flag bit is to be cleared.	Not used.
34—Control	Not used.	Q_8 and Q_9 specify input-output device. Q_{11} specifies control function to be performed.
35—Dump Numerically	Memory address from which first numerical character is to be written.	Q_8 and Q_9 specify output device.
36—Read Numerically	Memory address at which first numerical character is to be stored.	Q_8 and Q_9 specify input device.
37—Read Alphamerically	Memory address at which numerical digit of first character is to be stored. (Zone digit of first character will be stored at "P minus one.")	Same as Code 36.
38—Write Numerically	Memory address from which first numerical character is to be written.	Same as Code 35.
39—Write Alphamerically	Memory address for numerical digit of first character to be written. (Zone digit of first character is at "P minus one.")	Same as Code 35.
41—No Op	Not used.	Not used.
42—Branch Back	Not used.	Not used.
43—Branch On Digit	Memory address of the high-order digit of the next instruction to be interpreted and executed, if Branch occurs. (Not used if Branch does not occur.)	Memory address to be interrogated for the presence of a significant digit (not a zero).
44—Branch No Flag	Same as Code 43.	Memory address to be interrogated for the presence of a flag bit.
45—Branch No Record Mark	Same as Code 43.	Memory address to be interrogated for the presence of a Record Mark character.
46—Branch Indicator	Same as Code 43.	Q_8 and Q_9 digits specify program switch or indicator to be interrogated for status.
47—Branch No Indicator	Same as Code 43.	Same as Code 46.
48—Halt	Not used.	Not used.
49—Branch	Memory address of the high-order digit of the next instruction to be interpreted and executed.	Not used.
71—Move Flag	Memory address of flag to be moved.	Memory address to which flag is to be moved.
72—Transfer Numerical Strip	Memory address of the units position of the alphameric field.	Memory address of the units position of the numerical field.
73—Transfer Numerical Fill	Same as Code 72.	Same as Code 72.

* Immediate.

INSTRUCTION FORMAT



TYPEWRITER SPACING SCALE

IBM Reference Card | 1620 Data Processing System

SWITCH AND INDICATOR CODES

Q_b	Q_D	
0	1	Program Switch 1
0	2	Program Switch 2
0	3	Program Switch 3
0	4	Program Switch 4
0	6	Read Check Indicator*
0	7	Write Check Indicator*
0	9	Last Card Indicator
1	1	High-Positive Indicator
1	2	Equal-Zero Indicator
1	3	High-Positive or Equal-Zero Indicator
1	4	Overflow Check Indicator
1	6	MBR-Even Check Indicator*
1	7	MBR-Odd Check Indicator*
1	9	Any Data Check

* Will Cause 19 to be ON.

COMPARE RESULTS

Condition (Algebraic)	Indicator	
	High/Positive	Equal/Zero
P Greater Than Q	ON	OFF
P Less Than Q	OFF	OFF
P Equal to Q	OFF	ON

P = Data in Field at P Address
Q = Data in Field at Q Address

INPUT/OUTPUT DEVICE CODES

Q_A	Q_B	Device
0	1	Typewriter — 10 char/sec
0	2	Tape Punch — 15 char/sec
0	3	Paper Tape Reader — 150 char/sec
0	4	Card Punch — 125 cpm
0	5	Card Reader — 250 cpm

CORE STORAGE TABLE AREAS

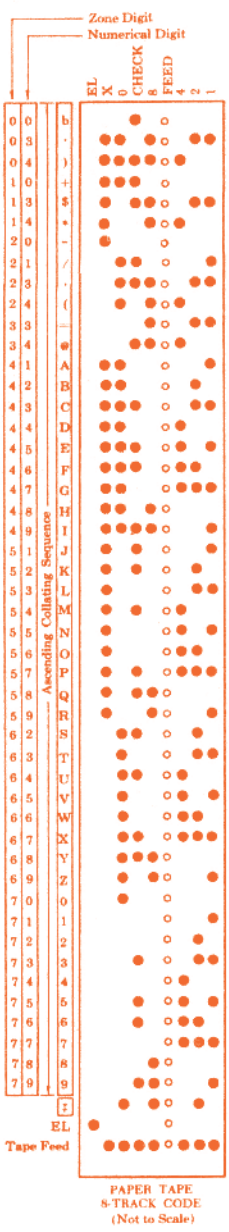
Address	Area
00000-00099	Console Area
00080-00099	Product Area
00100-00299	Multiply Table
00300-00399	Add Table

TYPEWRITER CONTROL CODES

Q_{13}	
1	Space
2	Return Carriage
8	Tabulate

BIT CODE, DECIMAL DIGITS 0-9

	C	F	8	4	2	1
0	1	0	0	0	0	0
1	0	0	0	0	0	1
2	0	0	0	0	1	0
3	1	0	0	0	1	1
4	0	0	0	1	0	0
5	1	0	0	1	0	1
6	1	0	0	1	1	0
7	0	0	0	1	1	1
8	0	0	1	0	0	0
9	1	0	1	0	0	1



PAPER TAPE
8-TRACK CODE
(Not to Scale)

PAPER TAPE SCALE

SIGN CONTROL CHART

	ADD				SUBTRACT			
Sign of P Field	+	+	−	−	+	+	−	−
Sign of Q Field	+	−	+	−	+	−	+	−
Stored P Field Sign	+	+	−	−	+	+	−	−
True or Complement Add Q Field	True	Comp	Comp	True	Comp	True	True	Comp
Recomplement Answer if Q Field Value is Greater Than P Field Value		X	X		X			X
Resulting Sign of P Field (Change on Recomplement)	+	−	+	−	−	+	−	+

Mnemonic	Code	Instruction	Operation	Time
A	21	Add	$F_P + F_Q$ replaces F_P	160 + 80 D_P, basic time 80 D_P, recomp. time†
AM	11	Add (I)	$F_P + Q$ replaces F_P	160 + 80 D_P, basic time 80 D_P, recomp. time†
B	49	Branch	Do I_P	200
BB	42	Branch Back	Do I_s	200
BD	43	Branch on Digit	If d_Q not zero, do I_P	200 No Branch 240 Branch
BI	46	Branch Indicator	If i_Q on, do I_P	160 No Branch 200 Branch
BNF	44	Branch No Flag	If no f_Q, do I_P	200 No Branch 240 Branch
BNI	47	Branch No Indicator	If i_Q off, do I_P	160 No Branch 200 Branch
BNR	45	Branch No Record Mark	If no r_Q, do I_P	200 No Branch 240 Branch
BT	27	Branch & Transmit	Save A_s, F_Q to $L_P - 1$, do I_P	200 + 40D_Q
BTM	17	Branch & Transmit (I)	Save A_s, Q to $L_P - 1$, do I_P	200 + 40$D_{Q'}$
C	24	Compare	F_P compared with F_Q	200 + 80D_z Unlike signs 160 + 80D_z Like signs
CF	33	Clear Flag	Remove f from L_P	200
CM	14	Compare (I)	F_P compared with Q	200 + 80D_z Unlike signs 160 + 80D_z Like signs
D	29	Divide	Product Area (00080-00099) ÷ F_Q	160 + 520$D_V$$D_Q$ + 740D_T Average quotient digit 4.5
DM	19	Divide (I)	Product Area (00080-00099) ÷ Q	160 + 520$D_V$$D_T$ + 740D_T Average quotient digit 4.5
DN	35	Dump Numerically	I/O_Q writes from L_P to 19, 999, 39, 999 or 59, 999	§
H	48	Halt	Stop	160
K	34	Control	Do Q_{11} on I/O_Q	¶
LD	28	Load Dividend	F_Q to L_P	400 + 40D_N
LDM	18	Load Dividend (I)	Q to L_P	400 + 40D_N
M	23	Multiply	F_Q x F_P (result at 00099)	560 + 40D_Q + 168$D_P$$D_Q$
MF	71	Move Flag	f_Q to L_P	240
MM	13	Multiply (I)	Q x F_P (result at 00099)	560 + 40$D_{Q'}$ + 168$D_P$$D_{Q'}$
NOP	41	No Operation	Go to A_s	160
RA	37	Read Alphamerically	I/O_Q reads at $L_P - 1$	§ Except Card I/O (3.4 ms)
RN	36	Read Numerically	I/O_Q reads at L_P	§ Except Card I/O (3.4 ms)
S	22	Subtract	$F_P - F_Q$ replaces F_P	160 + 80D_z basic time 80 D_P, recomp. time†
SF	32	Set Flag	Place f at L_P	200
SM	12	Subtract (I)	$F_P - Q$ replaces F_P	160 + 80D_z basic time 80 D_P, recomp. time†
TD	25	Transmit Digit	d_Q to L_P	200
TDM	15	Transmit Digit (I)	Q_{11} to L_P	200
TF	26	Transmit Field	F_Q to L_P	160 + 40D_Q
TFM	16	Transmit Field (I)	Q to L_P	160 + 40$D_{Q'}$
TNF	73	Transfer Numerical Fill	F_Q to F_P	160 + 40 D_P
TNS	72	Transfer Numerical Strip	F_Q to F_P	160 + 40 D_P
TR	31	Transmit Record	R_Q to L_P	160 + 40D_Q
WA	39	Write Alphamerically	I/O_Q writes from $L_P - 1$	§ Except Card I/O (3.4 ms)
WN	38	Write Numerically	I/O_Q writes from L_P	§ Except Card I/O (3.4 ms)

Symbols and Definitions for "Operation" Column			
P	P part of instruction	R_Q	Record defined by Q
Q	Q part of instruction	I/O_Q	I/O defined by $Q_A Q_B$
F_P	Field defined by P	d_Q	Digit at L_Q
F_Q	Field defined by Q	f_Q	Flag bit at L_Q
I_P	Instruction defined by P	f	Flag bit
I_s	Saved instruction	r_Q	Record mark at L_Q
L_P	Location defined by P	i_Q	Indicator defined by $Q_A Q_B$
L_Q	Location defined by Q	A_s	Address of next seq. instr.

Symbols and Definitions for "Time" Column	
D_P	Number of digits, including high-order zeros, in the field at P.
D_Q	Number of digits, including high-order zeros, in the field at Q.
$D_{Q'}$	Number of digits, including high-order zeros, in the Q part of the instruction.
D_N	Number of digits, including high-order zeros, in the dividend.
D_T	Number of digits, including high-order zeros, in the quotient.
D_V	Number of digits, including high-order zeros, in the divisor.
D_z	Number of positions compared until a digit other than zero is detected in either field.
All times are in microseconds (1 microsecond = 1/1,000,000 second).	

† Immediate.
† If signs initially unlike and numerical value of Q data greater than P data.
‡ If signs initially alike and numerical value of Q data greater than P data.
§ Depends on speed of I/O device and number of characters involved.
¶ Depends on control function and speed of I/O device.

IBM
International Business Machines Corporation
Data Processing Division
112 East Post Road, White Plains, New York

Form X26-6872-3
Printed in U.S.A.

GENERAL INFORMATION

1. Manufacturer: NCR - ELLIOTT
2. Fully transistorized
3. Price (basic system): £ 30,000
4. Large capacity storage
5. Input and output on paper tape, magnetic films, punched cards and teleprinter
6. Aplications: Science, research, engineering, commercial, banks, etc.
7. First delivery: 1959
8. Number of computers sold:
   — End of 1961 - 60
   — July of 1962 - 100
9. Automatic floating point

Central processor

Internal representation: Binary
Basic frequency: 166.5 Kc/sec
Word dimension: 12 decimal digits
1. Integers: $-2^{38} \leqslant A \leqslant 2^{38}-1$
2. Fractions: $-1 \leqslant A \leqslant +1-2^{-38}$
3. Floating point:
$$\pm 1.73 \times 10^{-77} \leqslant A < \pm 5.8 \times 10^{76}$$

Type of instruction: Single address (2 instructions each word)
Power (basic system): 0.8 KVA

Arithmetic unit (all automatics)

Type: serial
Additions and subtractions (12 Dec. digits): 576 microsec.
Jumps and decisions: 288 microsec.
Multiplications (12 Dec. digits): 864 to 12 096 microsec.
Divisions (24 ÷ 12 Dec. digits): 12 096 microsec.

Main store unit

Type: Ferrite core
Capacity:
1. 8 192 words
2. 98 304 Dec. digits
3. 327 680 bits.

Access time and B-line modification: Included on the operation times given
Word capacity: 38 bits + 1 sign + 1 parity

1. Input (paper tape)

Type: Photoelectric reader
5 to 8 channel paper tape
Input rates:
— Maximum: 450 char./sec.
— Binary tapes: About 300 char./sec.
— Decimal tapes: 25 - 430 char./sec.
Cards: 400 cards/min.

2. Output (paper tape)

Number of channels: 5 to 8
Speed: 100 Char./sec.
Cards: 100 cards/min.

Film handler units

Type: Magnetic film, 35 mm
Capacity (each spool):
1. 262 144 words
2. 3 145 728 decimal digits
3. 10 485 760 bits

Transfer rate: 7500 Dec. dig./sec.
Number of blocks per film spool: 4096
Number of words per block: 64
Number of tracks: 9
Length of film: 960 ft
Speed of film: 27.4 inches/sec

Programming systems

1. Autocode
2. Machinecode
3. Algol (Algebraic oriented language)

Units of the installation

1. Central Processor:
   — 8192 words
   — Automatic floating point
2. Power unit
3. Paper tape station (P. T. S.)
4. Tape reader
5. Tape punch
6. Binary keyboard
7. Creed equipment (off-line)